AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0034] with the following paragraph in order to remedy typographical errors:

[0034] In accordance with one variation of the present invention, bias voltages applied to the well regions of the transistors used in inverters 301_1-301_M can be controlled to control the delay of delay element 205_1 (See, Fig. 3). Similar control is also exercised over delay elements 205_2-205_N. For example, if p-channel FET ~~311~~ 310 is fabricated in an n-well region, and n-channel FET ~~312~~ 320 is fabricated in a p-well region, then a higher bias voltage applied to the n-well region and a lower bias voltage applied to the p-well region will result in a relatively small signal delay through the associated inverter 301_1. Conversely, a lower bias voltage applied to the n-well region and a higher bias voltage applied to the p-well region will result in a relatively large signal delay through the associated inverter 301_1. Thus, during high frequency operation, a high bias voltage is applied to the n-well region and a low bias voltage is applied to the p-well region. During low frequency operation, a low bias voltage is applied to the n-well region and a high bias voltage is applied to the p-well region.